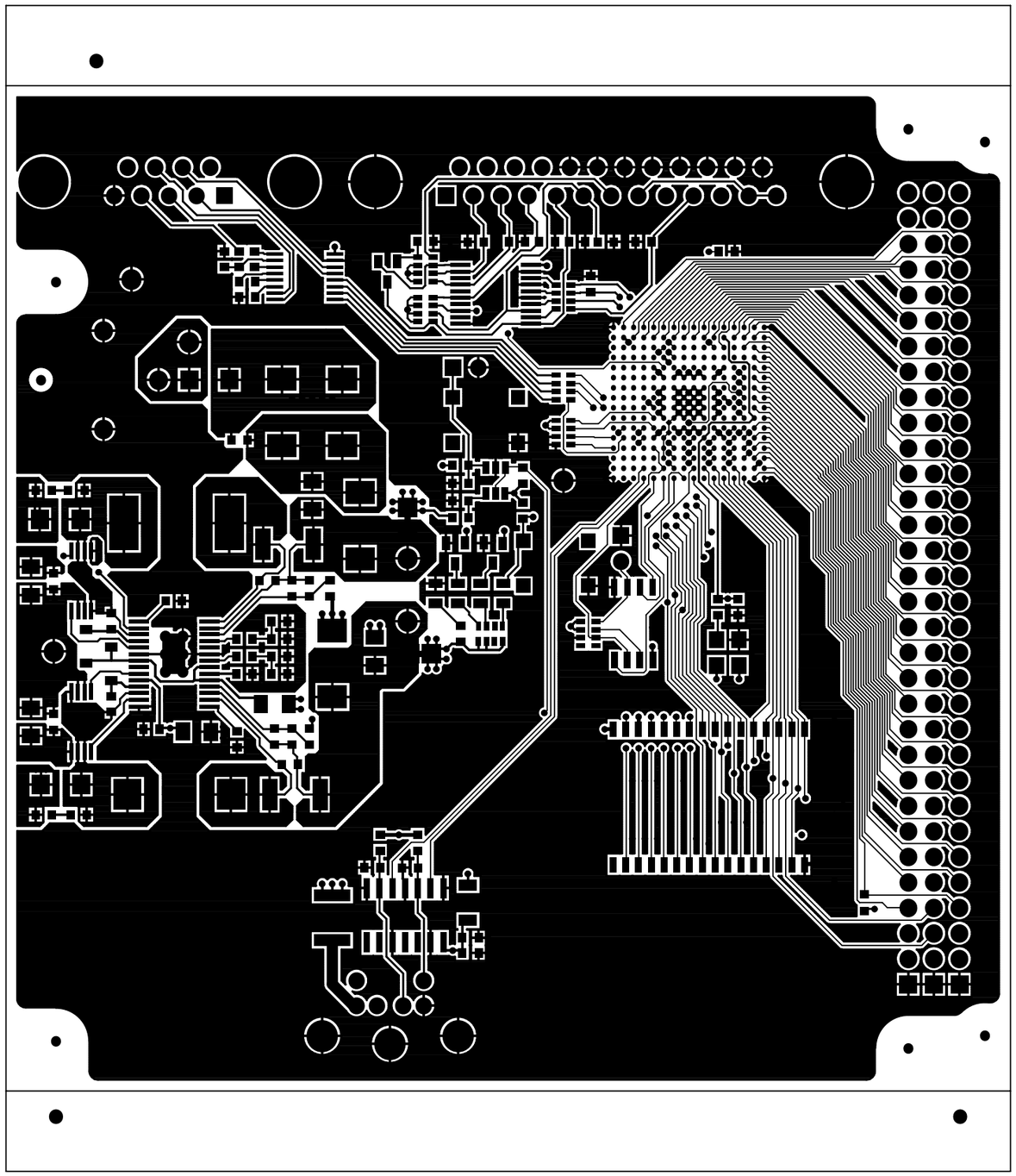
aq0181_diycalculator_fpga.PCBDOC

Top Layer .GTL

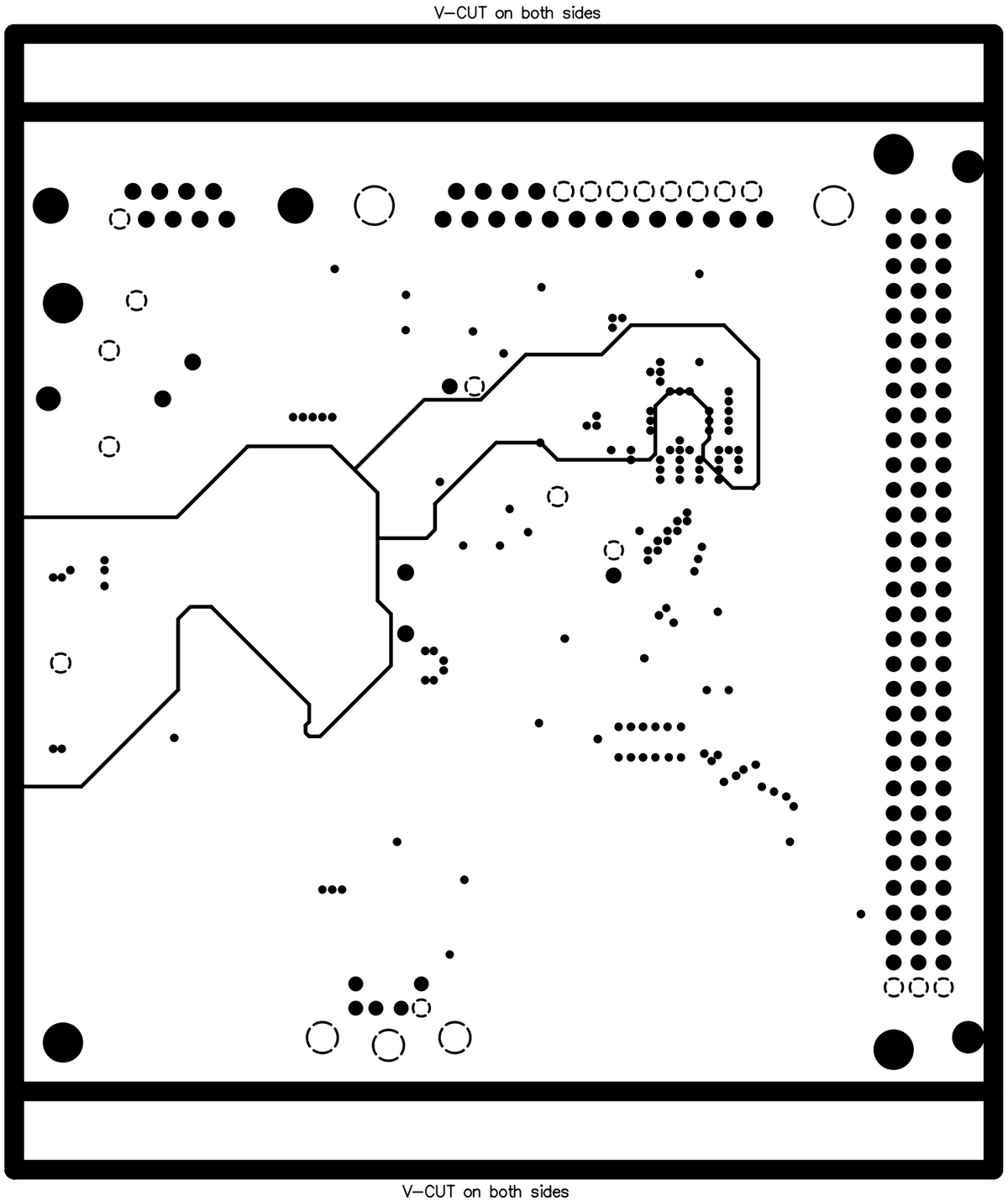
V-CUT on both sides



V-CUT on both sides

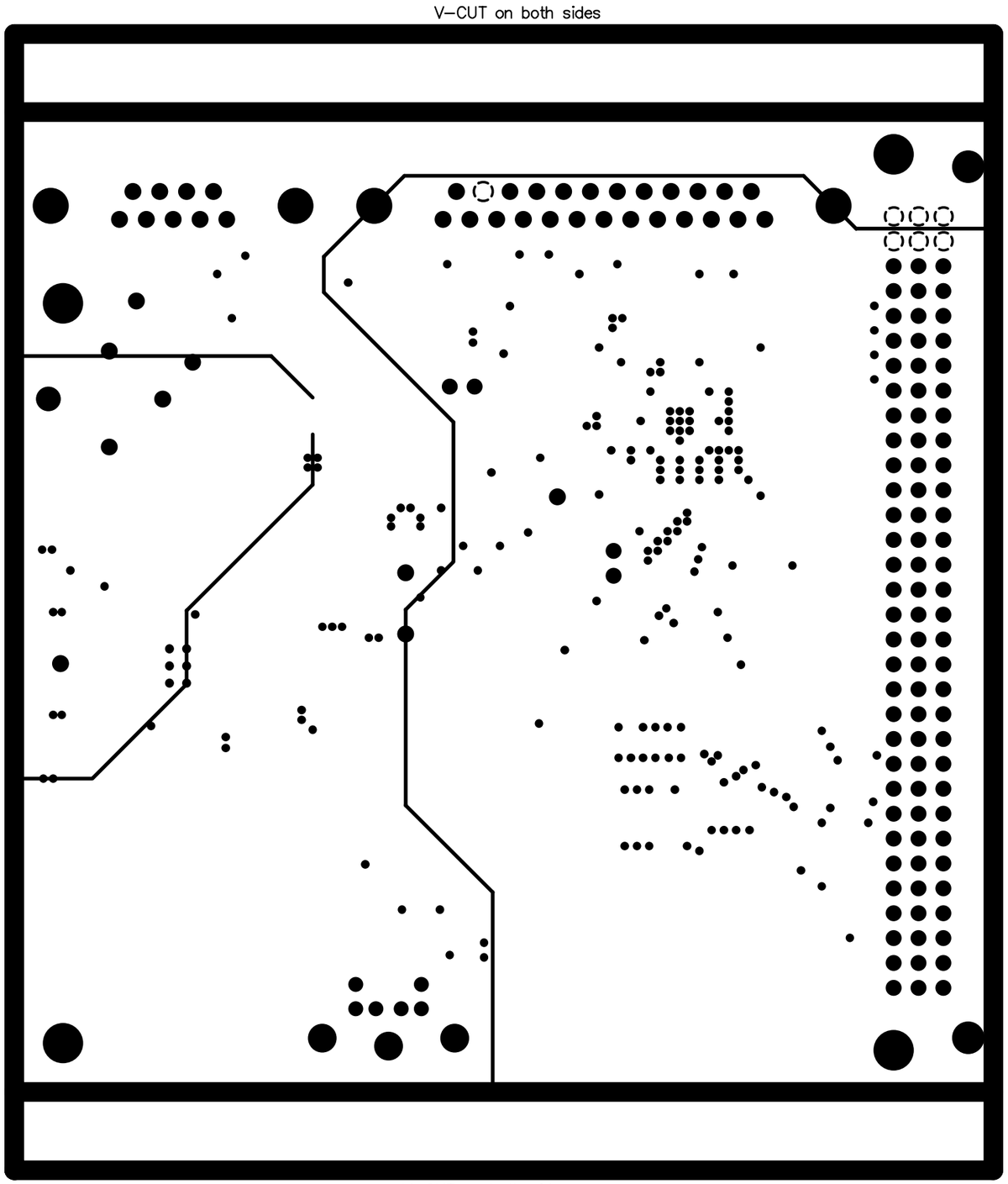
aq0181_diycalculator_fpga.PCBDOC

Internal Plane1 .GP1



aq0181_diycalculator_fpga.PCBDOC

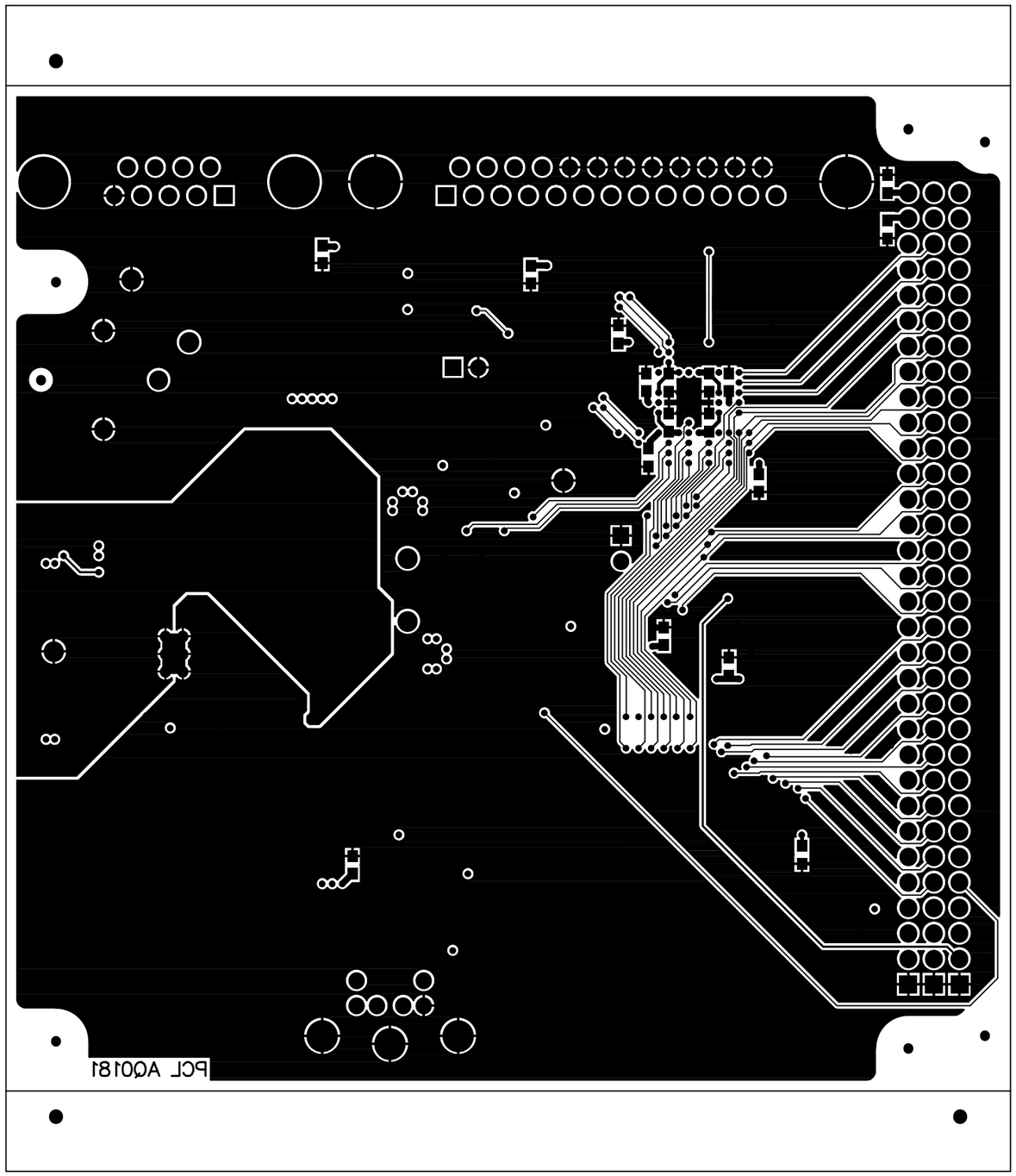
Internal Plane2 .GP2



aq0181_diycalculator_fpga.PCBDOC

Bottom Layer .GBL

V-CUT on both sides

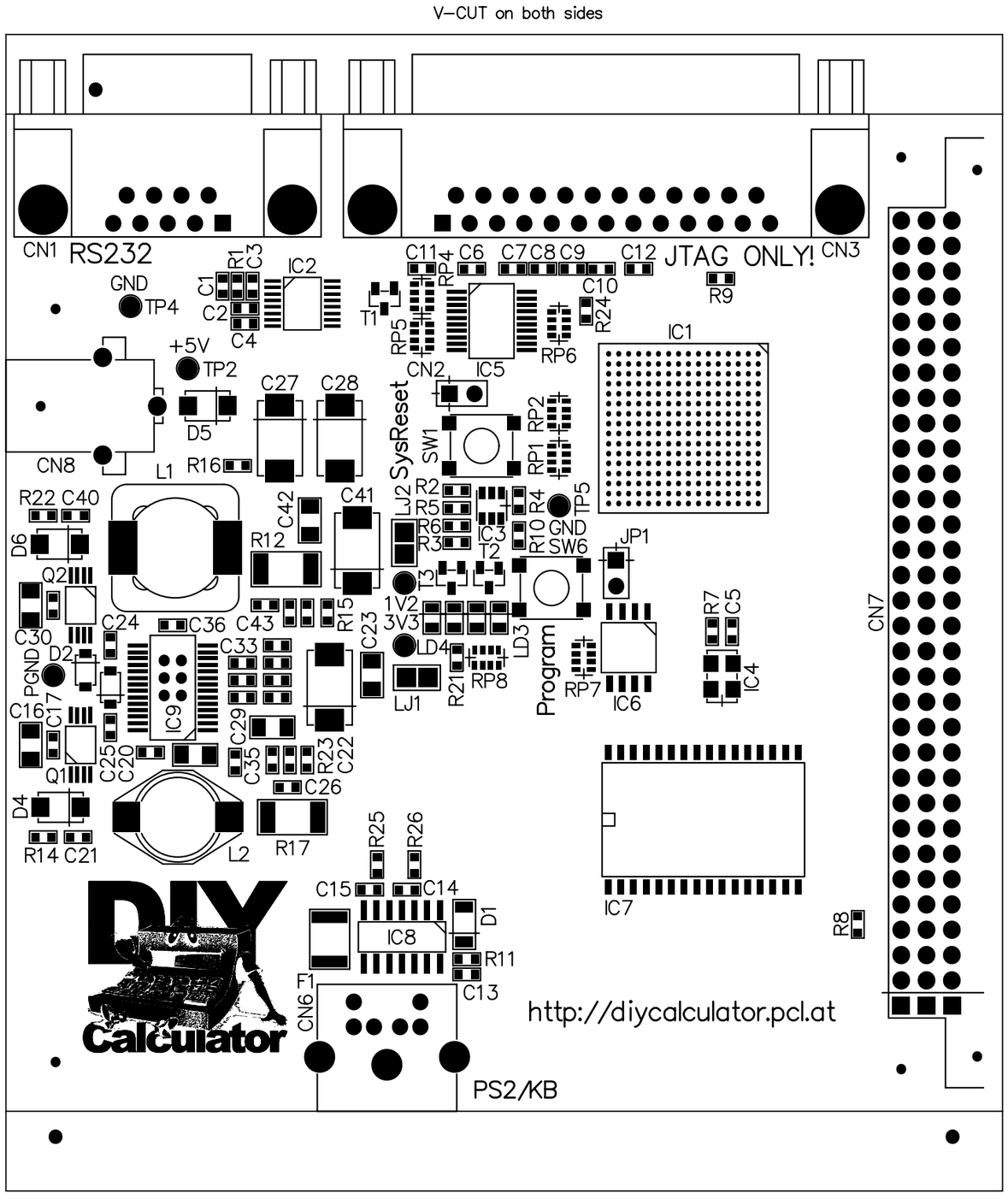


V-CUT on both sides

aq0181_diycalculator_fpga.PCBDOC

Top Overlay .GTO

V-CUT on both sides

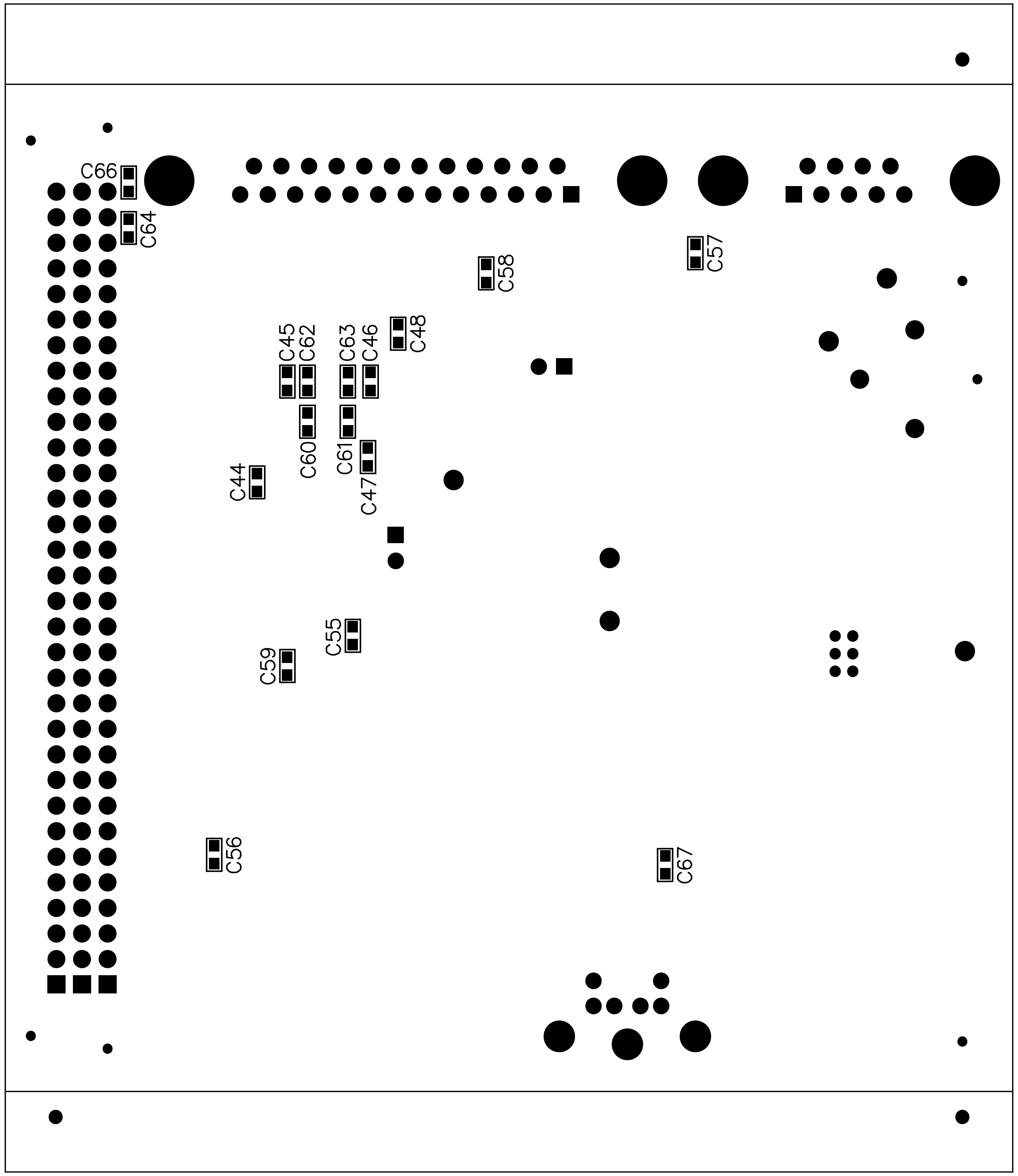


V-CUT on both sides

aq0181_diycalculator_fpga.PCBDOC

Bottom Overlay .GBO

V-CUT on both sides

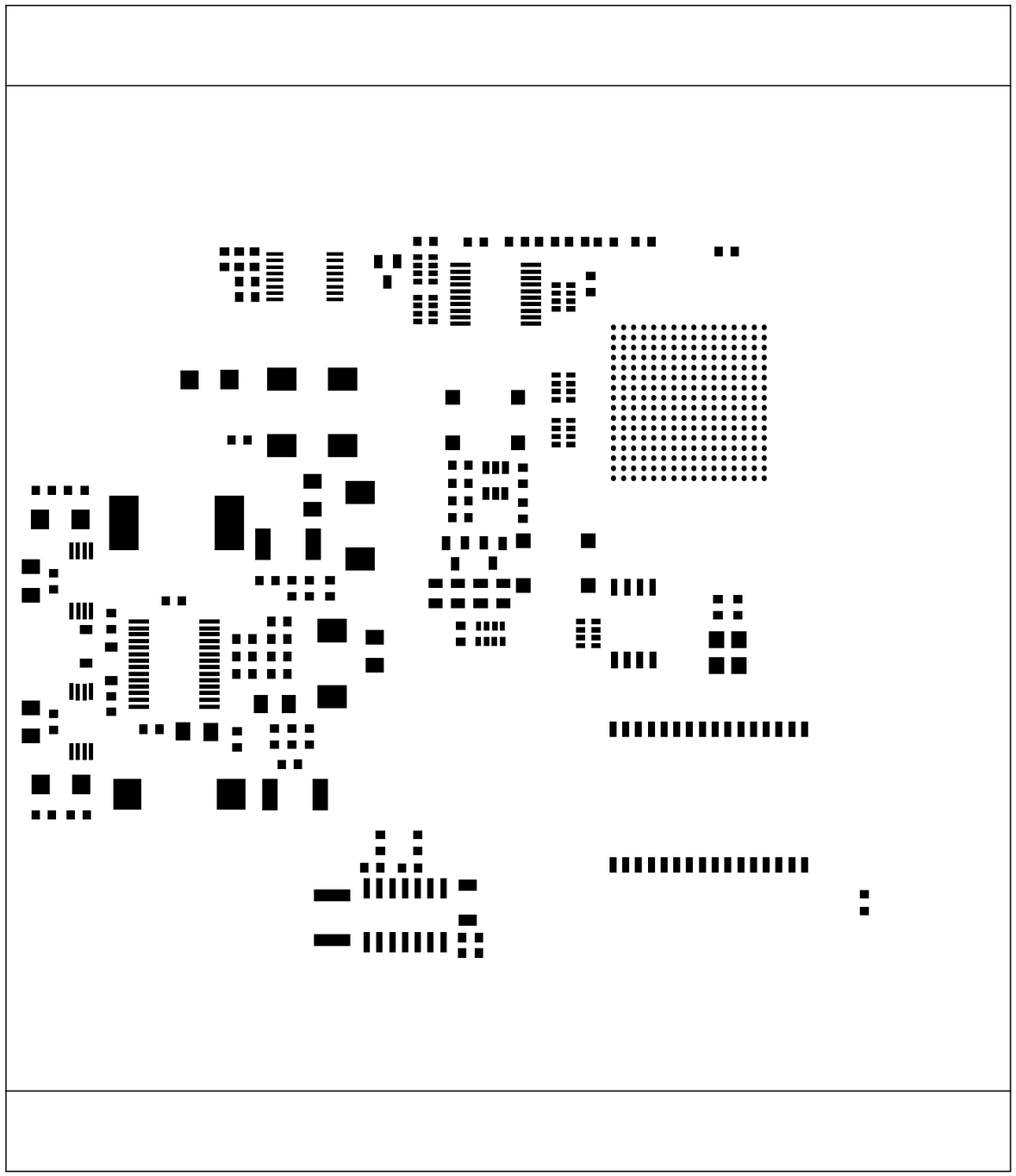


V-CUT on both sides

aq0181_diycalculator_fpga.PCBDOC

Top Paste .GTP

V-CUT on both sides

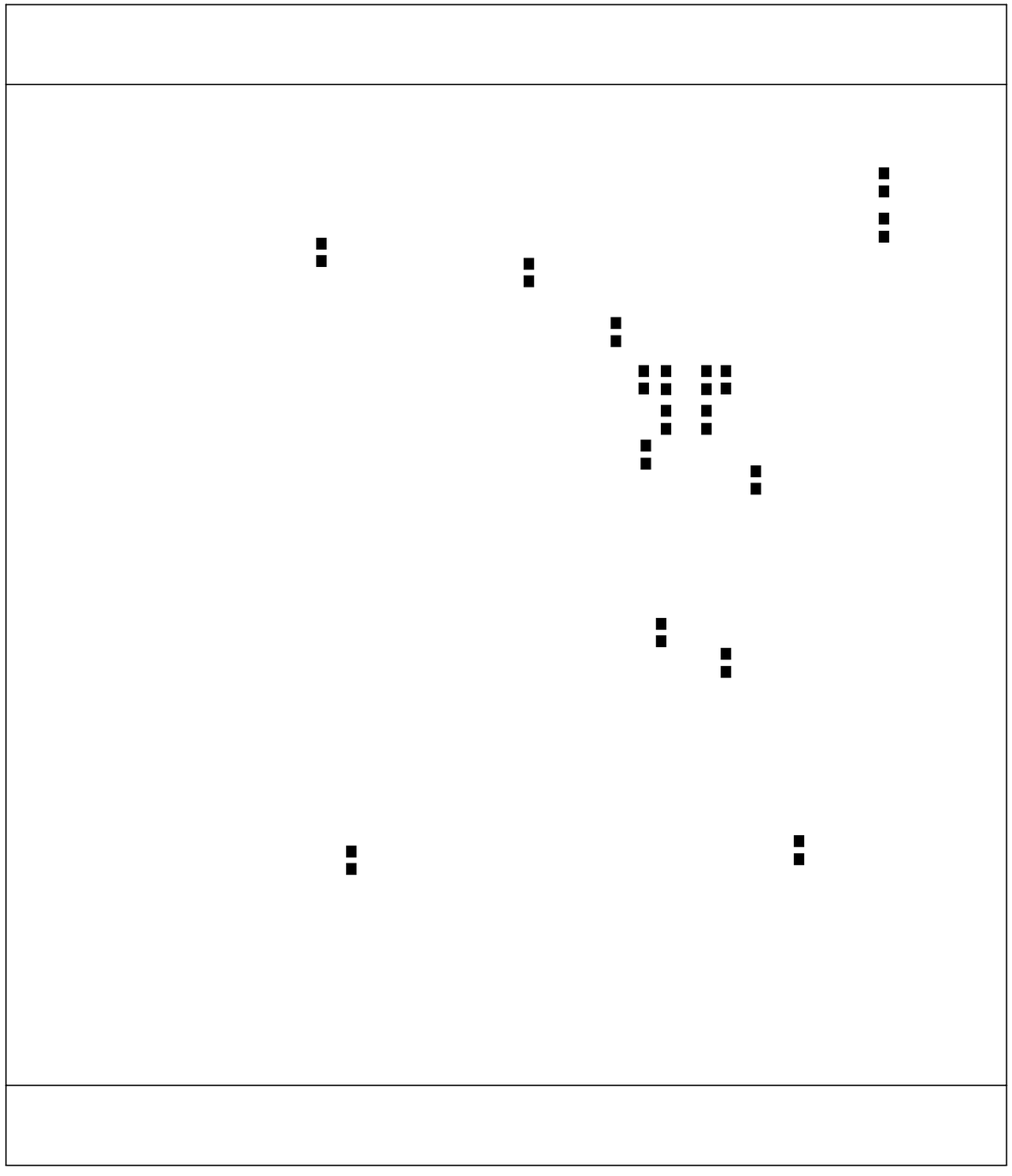


V-CUT on both sides

aq0181_diycalculator_fpga.PCBDOC

Bottom Paste .GBP

V-CUT on both sides

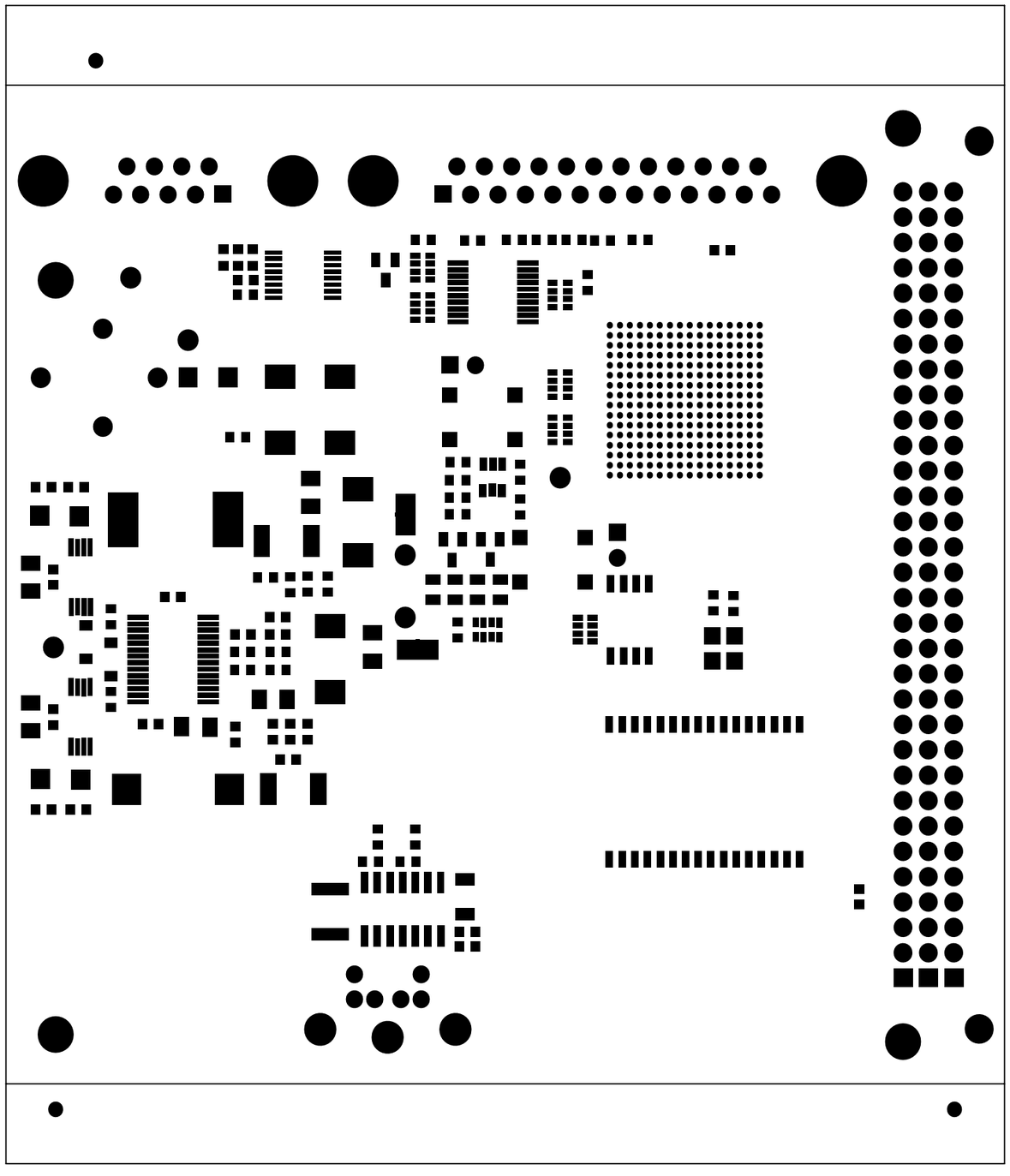


V-CUT on both sides

aq0181_diycalculator_fpga.PCBDOC

Top Solder .GTS

V-CUT on both sides

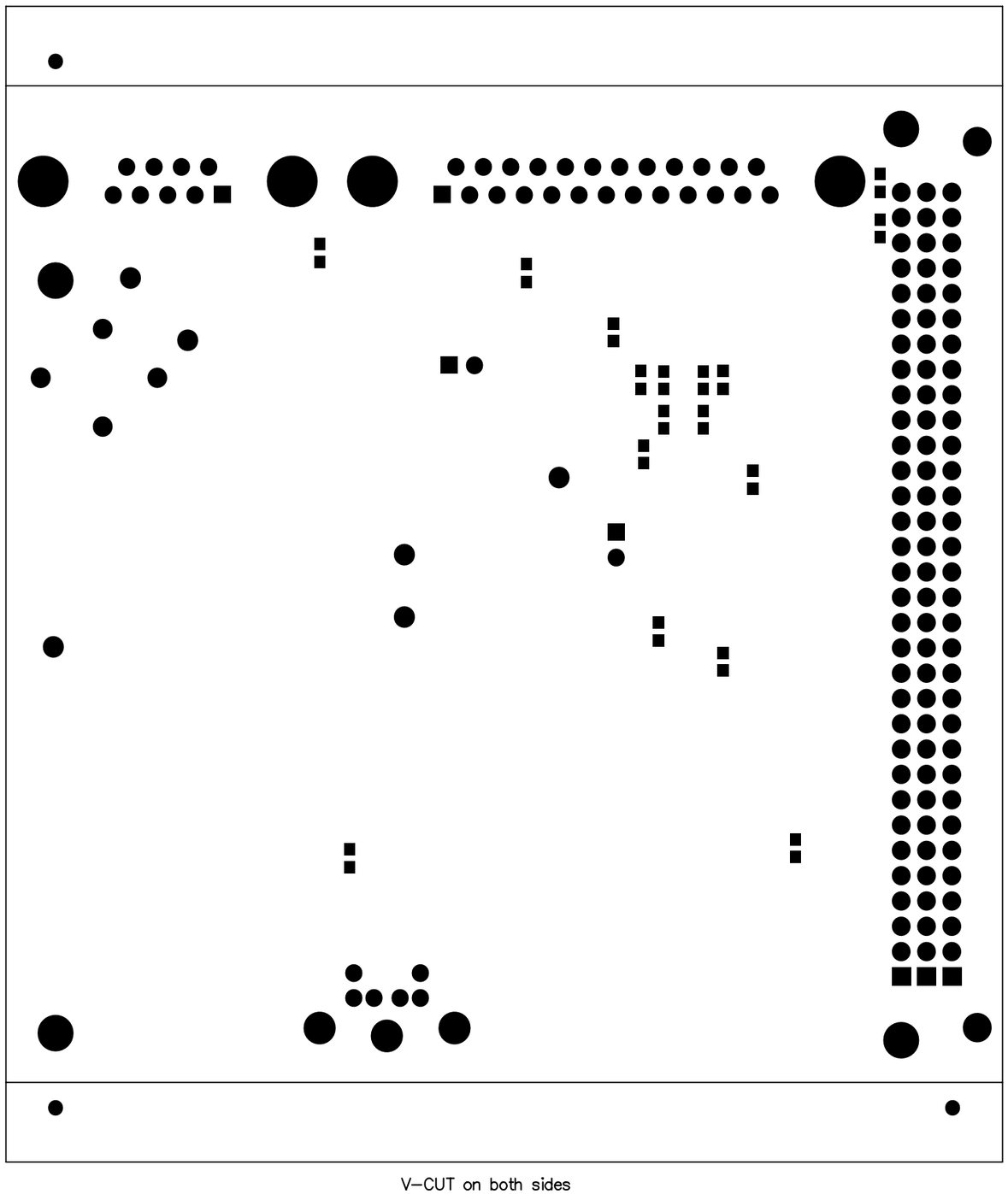


V-CUT on both sides

aq0181_diycalculator_fpga.PCBDOC

Bottom Solder .GBS

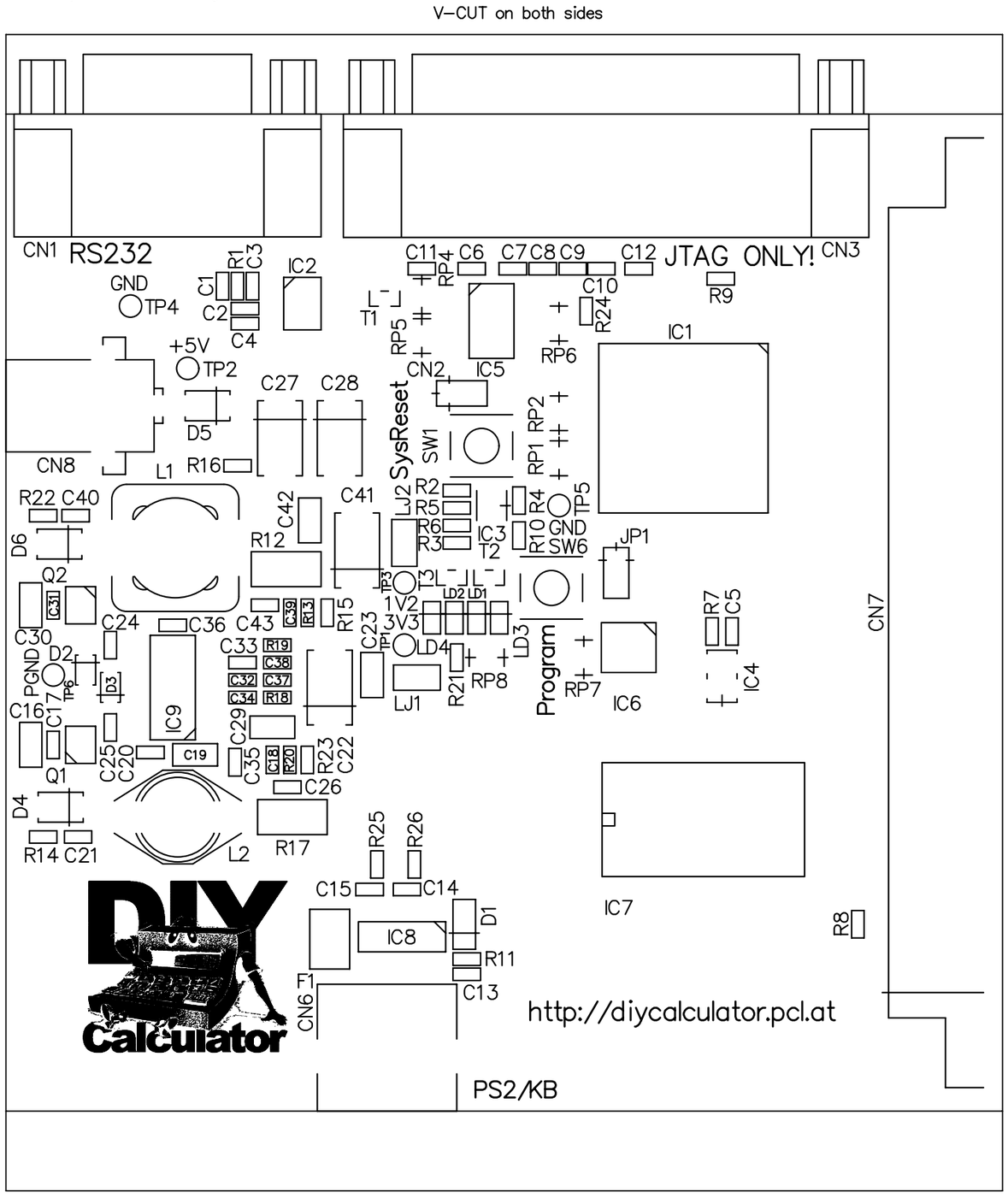
V-CUT on both sides



V-CUT on both sides

aq0181_diycalculator_fpga.PCBDOC

Top Overlay .GTO

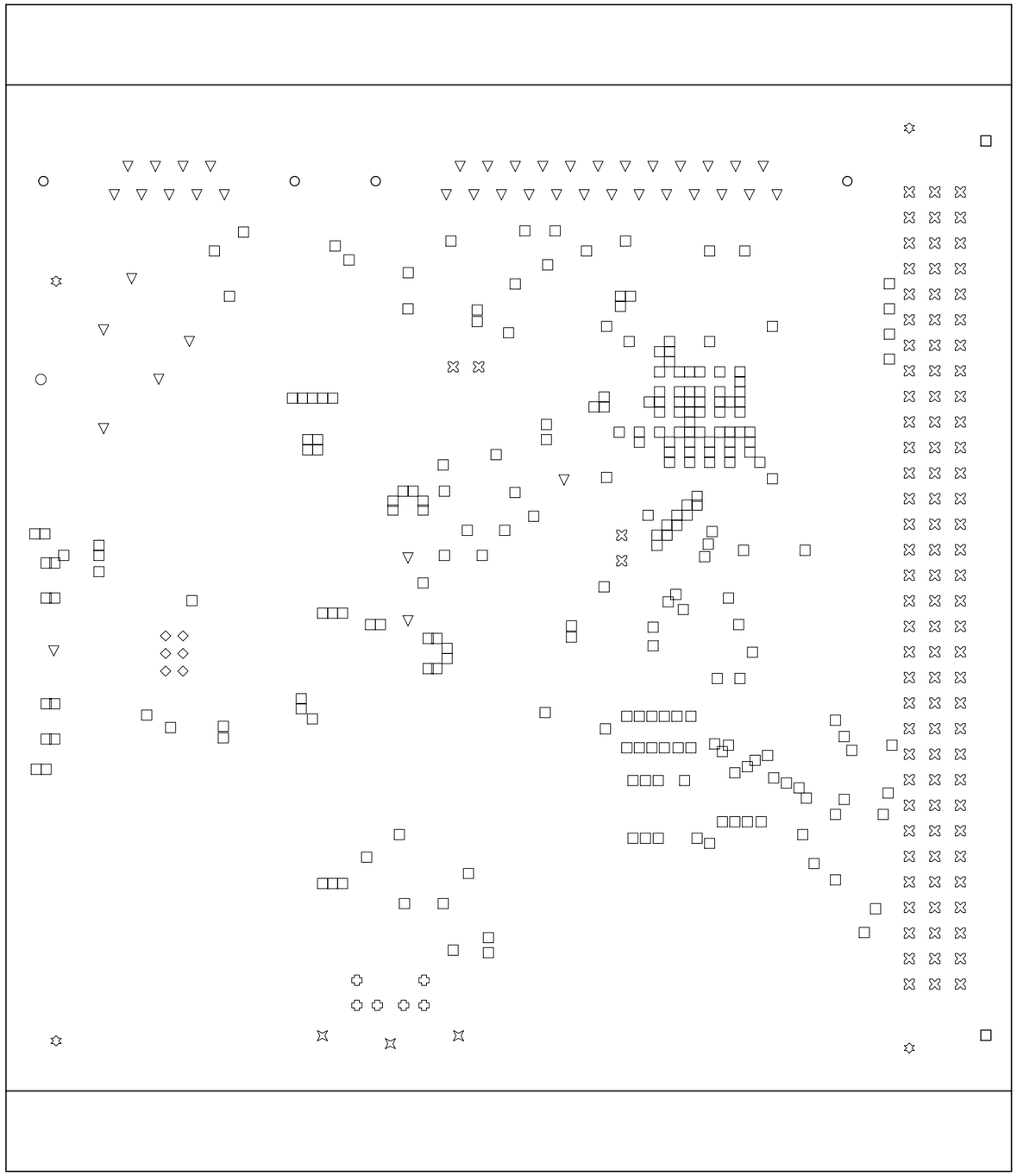


V-CUT on both sides

aq0181_diycalculator_fpga.PCBDOC

Drill Drawing .DRL

V-CUT on both sides



V-CUT on both sides

Layer Stack Up Detail for: aq0181_diycalculator_fpga.PCBDOC

Layer Name
Top Layer
InternalPlane1
InternalPlane2
Bottom Layer

FR4 / 1.6mm / 35u / Surface Sn

□	246	9.842mil	0.25mm	PTH	Round
◇	6	11.811mil	0.3mm	PTH	Round
⌖	6	35.433mil	0.9mm	PTH	Round
⊠	100	39.37mil	1mm	PTH	Round
▽	43	43.307mil	1.1mm	PTH	Round
○	1	74.803mil	1.9mm	NPTH	Round
⊠	3	90.551mil	2.3mm	PTH	Round
□	2	106.299mil	2.7mm	NPTH	Round
○	4	120.079mil	3.05mm	PTH	Round
☼	4	137.795mil	3.5mm	NPTH	Round
	415	Total			

Drilling Details